REMARKS

Claims 1-23 stands rejected under 35 USC §112, first paragraph, because the Examiner indicates that the specification is enabling only for a second clock frequency (read clock) or data width being selectively provided for outputting data and control information from a FIFO RAM with no back pressure, not both. Claims 1, 2, 6-9, 11, 13-18, 20-22 stand rejected under 35 USC §103(a) as being unpatentable over Hsu et al., U.S. patent publication US 2003/0177295 in view of Aipperspach et al U.S. patent publication US 2003/0128611. Claims 3, and 4 stand rejected under 35 USC §103(a) as being unpatentable over Hsu et al., U.S. patent publication US 2003/0177295 in view of Aipperspach et al U.S. patent publication US 2003/0128611 in view of Adamchick, U.S. patent 4,122,520. Claims 5, 10,1 9, and 23 stand rejected under 35 USC §103(a) as being unpatentable over Hsu et al., U.S. patent publication US 2003/0177295 in view of Aipperspach et al U.S. patent publication US 2003/0128611 in view of Lee, U.S. patent publication US 2004/0093443. Claim 12 stands rejected under 35 USC §103(a) as being unpatentable over Hsu et al., U.S. patent publication US 2003/0177295 in view of Aipperspach et al U.S. patent publication US 2003/0128611 in view of Lowe et al., U.S. patent 6,937,172.

Each of the independent claims 1 and 16 has been amended to more clearly state the invention. Reconsideration and withdrawal of the rejection of claims 1-23 under 35 USC §112, first paragraph, is respectfully requested. As amended, claim 1 recites one of said second clock frequency of said asynchronous read clocked logic and a data width of said FIFO RAM being selectively provided for outputting said data and

control information from said FIFO RAM with no back pressure with said second clock frequency being faster than said first clock frequency. As amended, claim 16 recites selectively providing one of said second clock frequency and a data width of the FIFO RAM for outputting said data and control information from the FIFO RAM with no back pressure with said second clock frequency being faster than said first clock frequency. The specification is enabling for claims 1 and 16, as amended. As set forth at page 5, lines 7-11 and 30-32:

In accordance with features of the preferred embodiment of the flow through asynchronous elastic FIFO apparatus 100, there is no back pressure on the RAM 102, for example, with the B-SIDE clock being faster than the A-SIDE clock, so the RAM only needs to be deep enough to cover the Gray code synchronization latches 110, 112. * * * The flow through asynchronous elastic FIFO apparatus 100 of the preferred embodiment is arranged so that the FIFO RAM 102 can always drain faster than it can be loaded so there is no back pressure.

The specification is enabling for claims 1 and 16, as amended, as set forth at page 6, lines 2-20:

For example, the A-SIDE could be a PCI Bus Control Engine that moves 8-bytes at 133 MHz and the B-SIDE could be internal logic running at 250 MHz.

If a design has the A-SIDE running faster than the B-SIDE, for example, if the A-SIDE PCI bus is running in PCI-X MODE2, 8-bytes at 266 MHz, then there are two options:

1. Double the B-SIDE clock frequency. In this case change from 250MHz to 500 MHz for the read address logic that pulls the data from the RAM 102, so there is no

back pressure.

2. Double the width of the RAM 102. In this case the RAM 102 is changed, for example, from 8-bytes of data to 16-bytes of data. Then the A-SIDE would load RAM 102 half as often (16-bytes at 133 MHz) and the B-SIDE could keep up (16-bytes at 250 MHz), so there is no back pressure.

The novel combination of the use of RAM 102, Gray code having a single bit change, and the dual synchronization latches 110, 112 across an asynchronous boundary with selected A-SIDE and B-SIDE clocks and selected RAM data width for no back pressure, and storing the multiple Control Fields in the FIFO RAM 102 enables effectively connecting multiple engines that run asynchronously.

Reconsideration of the claimed invention, as now recited in the independent claims 1 and 16, as amended, and as described in the specification, is requested. Applicants respectfully submit that, as amended, the independent claims 1 and 16 define the subject matter of the invention.

Independent claims 1 and 16, as amended, are believed to more clearly state the invention and withdrawal of the rejection of claims 1-23 under 35 USC §112, first paragraph, is respectfully requested.

Hsu et al., U.S. patent publication US 2003/0177295 discloses apparatus and method for controlling an asynchronous First-In-First-Out (FIFO) memory. The asynchronous FIFO has separate, free running read and write clocks. A number of n-bit circular Gray code counters are used to handshake the operation between read and write parts of the FIFO, wherein n is any integer more than one. Additional binary counters are used to accumulate the read and write overflows for the circular Gray code counters. When any circular Gray code counter is overflow, the read or write count is

transferred to the respective binary counter for recording the FIFO accesses. As set forth at paragraph 24:

[0024] FIG. 5 illustrates the asynchronous dual port FIFO 500 in accordance with the invention. The asynchronous dual port FIFO 500 comprises a dual port random access memory (RAM) 510. Input data are written into the RAM 510 through an input port (not shown) and a write pointer Wptr indicates a write address. Output data are read from the RAM 510 through an output port (not shown) and a read pointer Rptr indicates a read address. The FIFO 500 further comprises a pair of read and write parts with symmetrical implementation. Each part contains an FIFO status indicator (501, 502), a handshaking unit (503, 504), and an overflow controller (505, 506). The FIFO status indicator (501, 502) indicates the levels of the RAM 510 use in an FIFO pointer and the read or write pointer (see FIG. 8). The level of the RAM 510 use in the FIFO pointer can state the FIFO full with FULL (see FIG. 8) in the write part and the FIFO empty with EMPTY in the read part. Each pointer is a binary counter. The handshaking unit (503, 504) contains two n-bit Gray code counters and a synchronizing circuit (see FIG. 6), wherein n is any integer more than one. The synchronizing circuit can be an Flip/Flop. The overflow controller (505, 506) cooperates with the handshaking unit to obtain the performance of FIG. 4. As cited, the performance is identical to both read and write parts. For simplicity, the further description only gives to the write part as shown in FIGS. 6 to 8.

Aipperspach et al U.S. patent publication US 2003/0128611 discloses that space, power and performance are improved by a memory device having multiple

modes of operation for elastic data transfer. The memory device is comprised of first and second elastic store memory blocks, each containing 16 (18 bit) memory locations, and a write/read decoder. The first memory block receives write data from a first (18 bit) input data bus, and outputs two memory locations (36 bits) of read data onto a four memory location (72 bit) output data bus. The second memory block receives write data from multiplexed first and second (18 bit) input data buses and outputs two memory locations of read data onto the four memory location (72 bit) output data bus. The write address decoder receives a 5 bit write address, wherein the write address decoder will, as a function of a mode signal for effectively changing the address space for writing data, direct write data received at the data inputs of the first and second elastic store blocks to the correct memory locations. In one mode, data received on the first input data bus will get written to either the first or second memory, and, in another mode, data received on the first input data bus will be written to the first memory block and data received on the second input data bus will be written to the second memory block.

[0016] Elastic data transfer interface 200 may be configured to operate in one of two modes: (1) in a first mode, as a memory array of thirty-two, 18-bit addressable locations, and, (2) in a second mode, as a memory array of sixteen, 36-bit locations. The array configuration is set by the mode indicated by a LINKMODE signal. When the LINKMODE is set to logical zero, each of the memory locations in elastic store memories 205, 210 are addressed separately and the array is configured to store thirty-two 18-bit words. As shown in FIG. 2, when LINKMODE signal is set to logic zero,

addresses 235 indicate each of the memory locations within elastic store memory 205 are addressed as 0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28 and 30 from left to right, respectively, and addresses 240 indicate the sixteen locations in the second elastic store memory 210 are addressed as 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29 and 31 from left to right, respectively.

[0020] In a preferred embodiment, decoder 215 is capable of operating in a Double-Write (DBLW) mode. In the double-write mode, two consecutive address locations within elastic data transfer interface 200 are written at the same time. In this mode, two word lines within each of the memory locations 232 and memory locations 234 are active at the same time. When elastic data transfer interface 200 is operating in the 18-bit mode, the addressed memory location within memory locations 232, 234 is addressed along with the next consecutively addressed location. For example, in the 18-bit mode, a write to address "0" would write the data on bus 252 into memory location 225. Simultaneously, address "1" within addresses 240 would also be addressed (activated), enabling memory location 250 to be written by the same 18-bits on bus 252 via bus 254. Similarly, when elastic data transfer interface 200 is operating in the 36-bit mode, one of the location addresses 245 is addressed by a write operation, the next consecutive location address is also activated. So, for example, if the write address on bus 258 is addressed "0", an active DBLW signal on bus 260 would cause decoder 215 to enable the address locations 225 and 250 at address "0", and would also enable the next consecutively addressed locations 230 and 251 at address "1". This would cause the 18-bits representing the lower half of 36-bit word on bus 252 to be

written to locations 225 and 230 and the 18-bits representing the upper half of the 36-bit word on bus 256 to be written into locations 250 and 251. As will be appreciated, use of the Double-Write function enables the system software or operator to dynamically adjust the speed of writes to the elastic memory storage to adjust for discrepancies in read and write frequencies of the system.

Adamchick, U.S. patent 4,122,520 discloses a microcomputer controller for a printer, and apparatus for facilitating direct memory access to the microcomputer, includes a central processing unit (CPU) with a known set-up time at the beginning of each machine cycle. A memory, associated with the CPU, has an access time less than the CPU set-up time. A pair of three-state buffers are utilized on the address bus to, and the data bus to and from, the memory from each of the CPU and a direct memory access (DMA) port. A DMA control circuit is coupled to the three-state buffers to facilitate direct access to the memory, from the DMA port, during CPU set-up time intervals and also returns control of memory access to the CPU when the set-up, or synchronization, time interval ends. The microcomputer controller is utilized with additional memory, of the read-only type, and shift registers for realizing a printer controller capable of receiving print character data from the DMA port and causing that data to be printed as the associated symbol, indicia and the like, in a print font selected responsive to incoming data.

Lee, U.S. patent publication US 2004/0093443 discloses apparatus for effectively and economically receiving packet by eliminating temporal memory and controller. The apparatus includes; an inspection logic circuit for inspecting data units

as soon as arrived in order to find error included in the packet and generating control signals according to a result of inspecting data unit; a multiplexer for receiving data units and distributing the received data units as soon as the data units are arrived; and a plurality of FIFO memories for receiving the data unit, storing the data unit in corresponding one of FIFO memories and deleting or completing to store data units according to the control signals from the inspection logic circuit. The present invention can reduce manufacturing cost of the apparatus by eliminating a temporal memory and a memory controller for the temporal memory and can also reduce a processing time.

Lowe et al., U.S. patent 6,937,172 discloses a system for gray-code counting in an integrated circuit such as a programmable logic device uses a binary adder coupled to a binary counter output and to a selected binary offset value. The binary adder provides a binary sum that is converted to a gray code value by a binary-to-gray converter. The gray code value represents the binary sum output. FIG. 9D is a simplified flow chart of a method 990 for Gray-code counting in a programmable logic device. FIG. 8 illustrates an example of a circuit suitable for performing this method. A selected pointer offset binary value is added to a pointer count binary value to produce a binary sum (step 991). The binary sum is converted to a Gray-code value (step 992), and the Gray-code value is coupled to a first port of a multiplexer (step 993). The multiplexer output is coupled to a register input (step 994), and the register output is coupled (fed back) to a second port of the multiplexer (step 996). The pointer count binary value is incremented in response to a pointer increment signal to create an incremented Gray-code value (step 997), and the incremented Gray-code value is

coupled through the multiplexer when the pointer increment signal is asserted (step 998), and the register output is coupled through the multiplexer when the pointer increment signal is not asserted (step 999).

Applicants respectfully submit that independent claims 1, and 16, as amended, are patentable over the references of record including the Hsu et al. and Aipperspach et al. Independent claims 1, and 16 respectively recite a flow through asynchronous elastic first-in, first-out (FIFO) apparatus and a method for implementing multi-engine parsing and authentication with a flow through asynchronous elastic first-in, first-out (FIFO) apparatus including a FIFO random access memory (RAM) having a data input for receiving data and a data output for outputting said data; the FIFO RAM including a plurality of locations for storing a plurality of words, each word including a set number of bits.

The flow through asynchronous elastic first-in, first-out (FIFO) apparatus of independent claim 1 further define: a FIFO random access memory (RAM) having a data input for receiving data and control information and a data output for outputting said data and control information; write clocked logic for loading said data and control information to said FIFO RAM at a first clock frequency; asynchronous read clocked logic for outputting said data and control information from said FIFO RAM at a second clock frequency.

The method of independent claim 16 further define the steps of: loading data and control information to the FIFO RAM at a first clock frequency; outputting said data and control information from the FIFO RAM at a second clock frequency.

Only Applicants teach a flow through asynchronous elastic FIFO apparatus that passes data and control information through the asynchronous FIFO RAM. Thus, as only taught by Applicants, enabling other higher level functions, such as, interleaving multiple direct memory accesses (DMAs), and providing a clean abort/discard data function. (See page 5, starting at line 12 of the specification.) Neither Hsu et al., nor Aipperspach et al. provides any remote suggestion of loading control information into the FIFO RAM. Only Applicants teach, as set forth at page 7, starting at line 7 that data and control information are all stored into the RAM 102 instead of just data. An exemplary Data Field and a plurality of exemplary Control Fields are illustrated and described with respect to FIG. 3.

The above features of the flow through asynchronous elastic first-in, first-out (FIFO) apparatus and a method for implementing multi-engine parsing and authentication as taught and claimed by Applicants in independent claims 1, and 16, as amended, are neither disclosed, nor remotely suggested, in Hsu et al. and Aipperspach et al. Both Hsu et al. and Aipperspach et al. teach storing data and do not teach, suggest, nor provide any motivation for storing data and control information.

Thus, each of the independent claims 1, and 16, as amended, is patentable.

Dependent claims 2-15, and 17-23 respectively depend from patentable independent claims 1, and 16, as amended, further defining the invention. Each of the dependent claims 2-15, and 17-23 is patentable.

Applicants have reviewed all the art of record, and respectfully submit that

the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-23, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

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